High frequency inverter including a boost chopper

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Abstract

This paper presents a new high frequency inverter for high power induction heating applications under a low utility voltage condition. This inverter realizes 2 functions in same time. One is a boost chopper function and other is a full bridge inverter. The boost chopper function of this inverter raises the DC bus voltage than an input voltage. Herewith, the boost chopper and one bridge realize an operation same as the full bridge inverter and a DC voltage is energized to the load resonant circuit positive and negative in turn. As this full bridge inverter operates under high DC bus voltage, the proposed inverter achieves high power without changing the input voltage to high. The proposed inverter has 6 switching modes including the voltage commutation mode for soft switching. The soft switching operations of S1 and S2 are obtained by connecting a small capacitor to S2 in parallel.

Furthermore, the design rule of resonant capacitance is explained for tuning the resonant frequency appropriate by using some simple equations. Additionally, the maximum rated power also can be estimated by them, and it is verified by a simulation. The experimental results using a scale model of proposed inverter achieved about 3.2 times output power than the conventional full bridge inverter in a same load condition.

1. Introduction

An induction heating technology has been applied to not only various industrial applications but also a lot of large cookers for business use. The output frequency is about 20 to 30 kHz in general, although its frequency range is different by the difference in a material of the cooker. The power range is several kW to 30kW in almost cases. The utility line voltage of the large cooker is 3 phase 200V in Japan. In addition, half-bridge inverter or full-bridge inverter is used for high frequency power supply. Particularly, the full-bridge inverter is often used when the required power is high.

Recently, it is required to develop the larger and higher-power IH cookers for business use. To realize it, a high power inverter is necessary. There are some ways to make the power of inverter large, and the best way is to change the utility voltage into high voltage. If the condition of the load resonant circuit is same, the output power becomes quadruple by doubling the input voltage easily. It is necessary to modify by the electric power receiving equipment in order to change the utility voltage in this case. However, there are many cases that modifying the electric power receiving equipment is very difficult in the actual use condition because of cost and space. On the other hand, the high power can be obtained by lowering the equivalent resistance of the induction heating load. For example, the output power is doubled by decreasing the equivalent load resistance into half. As discussed in more detail below, however, there is a problem that the power conversion efficiency declines.

In addition, these are a solution for high power that high frequency power supplying system employs a boost chopper except the high frequency inverter. It is so called 2 converter systems. But it is inevitable that the power conversion efficiency declines, because 2 converter systems have a lot of power devices and the conduction loss increases on the power devices.

This paper presents a novel high frequency inverter that the high power is obtained without changing the input voltage and equivalent resistance of the induction heating load. The proposed inverter has just 3 IGBTs and 1 DIODE. Therefore the main circuit configuration is simple. In this paper, the switching modes are described. The circuit simulation is implemented to estimate the principle of inverter's operation. Furthermore, a scale model is produced experimentally. The experimental measurement results demonstrate the theoretical analysis and the simulation results.

2. Proposed high frequency inverter and its switching pattern

2.1 Circuit configuration

Fig. 1 shows a main circuit of proposed high frequency inverter circuit including the boost chopper as a function. The circuit consists of 3 IGBTs, one output diode, a boost inductor Ld, an equivalent resistor Ro of the induction heating load, an equivalent inductor Lo, a series resonant capacitor Co, an loss-less snubber capacitor Csn, and a DC bus capacitor Cd of conventional inverter.

Ld-Sa-Da works like a boost chopper in this inverter. Therefore this part in the inverter can raise the voltage of the Cd than input voltage Ein. S1 and S2 receives the voltage of Cd, and they turned on and off alternately. This circuit resembles a system that consists of SEPP (Single Ended Push Pull) high frequency inverter with a series resonant load and a boost chopper circuit. However, its operation has a common point with the full bridge inverter. Sa works not only as the boost chopper switch but also as the inverter circuit and its operation synchronizes with S1. When Sa and S1 turn on, the output voltage becomes negative DC bus voltage: $-v_{Cd}$. In the mode that Sa and S1 are off state and S2 is on state, the stored magnetic energy in Ld is discharged through Da. Then Da and S2 becomes on state. Consequently the output voltage becomes positive DC bus voltage: $+v_{Cd}$. As a result, it is thought that the operation of this inverter is the same as full bridge inverter, because a DC voltage is energized to the load resonant circuit positive and negative in turn.

Therefore, it can be said that the proposed inverter is a pseudo-full bridge inverter which receives the high DC bus voltage of Cd provided by boost chopper function in the inverter. The number of switching devices are less than conventional full bridge inverter which includes 4 switching devices. So the inverter including the gate-drive circuit can be simplified.

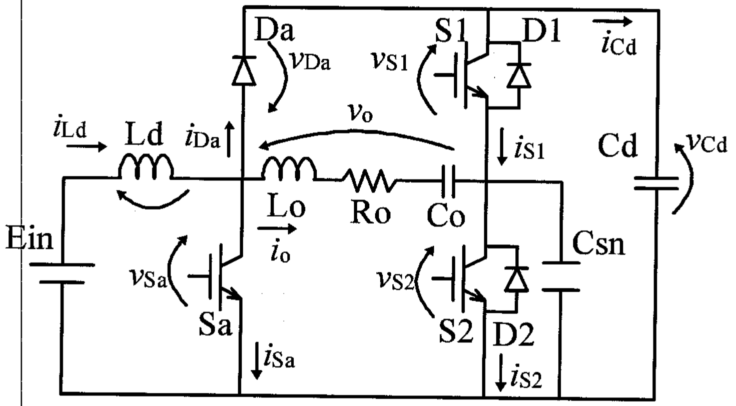

Fig. 1: A main circuit topology of the proposed high frequency inverter including a boost chopper function

2.2 Switching pattern

Fig. 2 shows the operation waveforms of proposed inverter. There are six operation modes in one cycle. The gate pulse signal v_{G1} is supplied to Sa and S1, and v_{G2} is given to switch S2. Td is a dead time to prevent short circuit of S1 and S2. The phase of the load current i_o delays compared to the output voltage v_o because this inverter operates in a little higher frequency band than the resonant frequency fr which is given by the load equivalent inductor Lo and the series resonant capacitor Co. S1 and S2 achieve ZVZCS (Zero Voltage Zero Current Switching) turn on naturally. The ZVS turn off of S1 and S2 is possible by connecting a small capacitor Csn in parallel. Fig. 3 illustrates the equivalent circuits of each switching mode. The operation modes of this inverter are explained based on Fig. 3.

(1) Mode 1 : Mode 1 starts by supplying v_{G1} to Sa and S1. The load current i_o flows through D1 to Cd. Input voltage Ed is applied to Ld, then i_{Ld} is increased.

(2) Mode 2 : Mode 2 starts when the load current direction changes into negative. S1 and Sa become on state. The stored energy in Cd is discharged through the load. The boost current flows through Ld as Ed is still applied to i_{Ld}. The current of i_{Sa} changes like a sinusoidal wave because the resonant load current also flows through Sa. The voltage across Da and S2 are equal to the voltage of Cd.
(3) Mode 3 : When Sa and S1 turn off, the inverter operation turns into Mode 3. An electric charge of Csn is discharged by current flowing through the load. In this period, voltage v_{S2} across S2 decreases by degree, and voltage v_{S1} across S1 rises to v_{Cd} at the same time. Therefore, S2 achieves a ZVS turn-off condition.
(4) Mode 4 : When an electric discharge of Csn is finished, mode 4 begins. The magnetic energy which has been charged in Ld during mode 1 and 2 discharges as current. The current flows though Da, then Cd is charged. As the load current still flows negative direction in this mode, D2 becomes on state. Gate signal voltage v_{G2} is given to S2 during this mode.
(5) Mode 5 : The load current turns into positive by the series resonance and the switching state becomes mode 5. The load resonant current flows through S2. The current waveform flowing through Da is difference of i_{Ld} and i_o.
(6) Mode 3 : When S2 turns off, a current flowing through the load charges Csn. S2 achieves a ZVS turn off as v_{S2} rises to v_{Cd} from zero by degree.
(7) Mode 6 : Mode 6 starts when the voltage of Csn reaches v_{Cd}. In this mode, not only i_{Ld} but also i_o flows into Cd, then the voltage across Cd becomes high. This mode continues during the dead time.

Proposed inverter can supply high frequency current to the load by repeating these six switching modes in order.

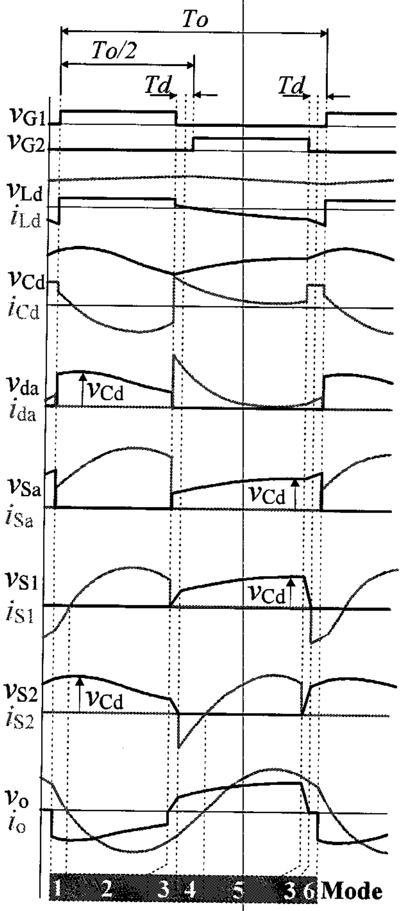

Fig. 2: The voltage and current waveforms in a steady operation

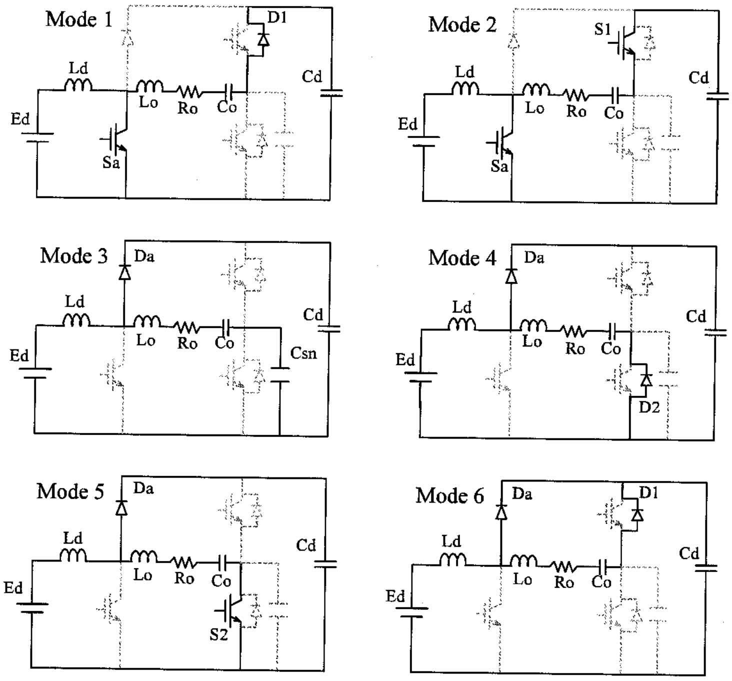

Fig. 3: Equivalent circuit of each switching operation mode

3. Circuit design

3.1 Design of the resonant capacitor Co

The induction heating load consists of a work coil and a metal cooker. And its equivalent circuit is represented by a series circuit of the equivalent inductor Lo and equivalent resistor Ro. The resonant frequency is determined by the equivalent inductor Lo and the resonant capacitor Co. The operation frequency of the proposed inverter is higher than the resonant frequency, which delays the phase of the output current to output voltage. Thus S1 and S2 achieve ZVZCS turn-on condition easily. The phase delay angle θ is given by the following equation.

$$\theta = \omega_o T_\theta \qquad \cdots(1)$$

where $\omega_o = 2\pi fo$, T_θ is the delay time of the load current to the output voltage, and fo is the operation frequency. Assuming that the load current and the output voltage are sinusoidal wave, the phase delay angle θ can be considered as a power factor of the series load resonant circuit. Therefore T_θ is given as follows.

$$T_\theta = \frac{\theta}{\omega_o} = \frac{1}{\omega_o}\tan^{-1}\frac{\omega_o Lo - \dfrac{1}{\omega_o Co}}{Ro} \qquad \cdots(2)$$

In addition, T_θ must be longer than dead time Td which prevents the short circuit of the semiconductor switch so that S1 and S2 achieve the ZVZCS turn-on condition by the current resonance.

$$T_\theta \geq Td \qquad \cdots(2)$$

Hence, the series resonant capacitor Co satisfying the condition of (3) is given by following equation.

$$Co \geq \frac{1}{\omega_o\left(\omega_o Lo - Ro\tan\omega_o Td\right)} \qquad \cdots(4)$$

Actually, the inverter output current does not become sinusoidal wave because the output voltage is similar to square wave. For this reason, the series resonant capacitance Co should be designed large a little so that the phase delay time of T_θ is long enough.

3.2 An estimate of the rated power

The output voltage of the boost chopper is given in the following equation.

$$Ed = \frac{1}{1-D}Ein \qquad \cdots(5)$$

where Ed is average voltage of DC bus capacitor Cd, Ein is input DC voltage to the inverter, and D is duty of the boost chopper switch Sa. The pseudo-full bridge inverter which consists of Da, Sa, S1 and S2 operates under this DC average voltage Ed. RMS value of fundamental wave V_1 that is included in the inverter output voltage is given in the following equation by Fourier series expansion.

$$V_1 = \frac{2\sqrt{2}}{\pi}Ed \cong 0.9Ed \qquad \cdots(6)$$

The inverter output current is given in the following equation by using the impedance Z of series resonant circuit.

$$I_o = \frac{V_1}{|Z|} = \frac{V_1}{\sqrt{Ro^2 + \left(\omega_o Lo - \dfrac{1}{\omega_o Co}\right)^2}} \qquad \cdots(7)$$

Therefore, rated output power Po-max of the inverter is given in the following equation.

$$P_{o-max} = I_o^2 Ro \cong \frac{0.81 Ed^2 Ro}{Ro^2 + \left(\omega_o Lo - \frac{1}{\omega_o Co}\right)^2} = \frac{0.81(1-D)^2 Ein^2 \frac{1}{Ro}}{1+\tan^2\theta} \quad \cdots(8)$$

3.3 The equivalent load resistance of the induction heating load

As mentioned before, the load equivalent resistance Ro effects the rated output power of the high frequency inverter except the input DC bus voltage. The rated power Po-max increases in proportion to Ro (refer equation 8). Therefore high power is obtained by decreasing Ro. Precise equivalent circuit of induction heating load is represented as a transformer's T type circuit. The work coil is primary side and the pan is secondary side. The gap between the work coil and the pan is related to an electromagnetic coupling. The mutual inductance decreases and the leakage inductance increases when the gap is large. A real part of the equivalent transformer circuit which represents the induction heating load decreases when the mutual inductance decreases. Consequently the value of Ro can be decreased by expanding a gap between a work coil and a cooking device.

For example, Fig. 4 shows a sample of relationship between the gap and the equivalent resistance Ro of the induction heating load that is used for a scale model in experiment. The equivalent resistance Ro can be measured by imputing several 100W into the induction heating load. In addition, it is possible to lower the equivalent load resistance by reducing the turns of work coil. However, reducing Ro leads to increase an exciting current in primary side, which increases the copper loss of the work coil.

Therefore it should be noted that the temperature of the work coil tends to be high and the efficiency of the induction heating load becomes low if Ro is adjusted to low in order to obtain high power. In any method to reduce Ro, not only Ro but also the equivalent inductance Lo is changed at the same time. Generally, Lo is proportional to the turns of work coil and inverse proportion to the gap between the work coil and the cooking device.

Therefore, the design method of this high frequency inverter is recommended to decide the phase delay angle θ on the basis of equation (1) after deciding the delay time T_θ and the operation frequency fo. Next the proper equivalent resistance Ro should be known so that the inverter output a requested maximum power Po-max. Ro can be calculated by the input DC voltage Ein, the duty factor D of Sa, and Po-max on the basis of equation (8). It is easy to adjust the equivalent resistance by changing a length of the gap of between the cookers and the work coil of induction heating load. The equivalent inductor Lo is also determined inevitably when Ro is set. Finally the proper resonant capacitance Co is grasped easily by equation (4).

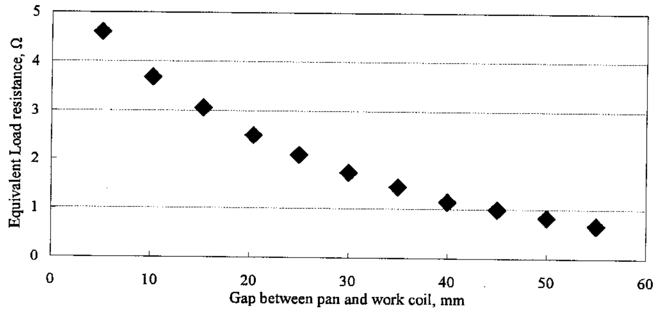

Fig. 4: An example of the changing trend of equivalent load resistance to the gap

4. The evaluation of the proposed inverter circuit

4.1 A scale model

A scale model of proposed high frequency inverter is designed to evaluate itself. Fig. 5 shows an induction heating load used for the scale model. The work coil consists of a litz wire for reducing the power loss by skin effect. The coil diameter is about 268mm. An iron pan is used as induction heated load and its diameter is about 295mm.The gap between the coil and the pan is adjusted to 12mm by putting the insulating material between those.

The operation frequency fo and the dead time are set as fo=22kHz, Td=2µs. As described in equation (3) T_θ have to be long than Td for realizing the ZVS operations of S1 and S2. Then T_θ is set around 4µs. Therefore the resonant capacitor is decided to Co=1.8µF on a basis of equation (8). From the above, a each parameter of the scale model is decided as shown in Table 1.

Table 1: Specification of scale model

Components	Symbol	Value	Unit
Equivalent Load Inductor	Lo	42	µH
Equivalent Load Resistor	Ro	3.5	Ω
Series Resonant Capacitor	Co	1.8	µH
DC Bus Capacitor	Cd	6	µH
DC Reactor	Ld	128	µH
Loss-less Snubber Capacitor	Csn	47	nF
Input DC mean Value	E_{in}	50	V
Operation Frequency	f_o	22	kHz
Dead Time	T_d	2	µs

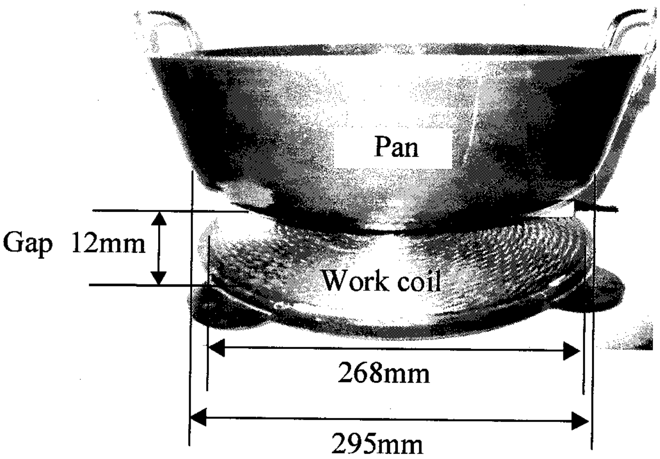

Fig. 5: The scale model condition of the induction heating load

4.2 The evaluation analysis of the output power

Equation (8) says that the proposed inverter's rated power is determined by the duty factor of v_{G1} that is supplied to Sa. If the rated power is obtained when the duty factor of the gate signal v_{G1} and v_{G2} are 0.5 without the dead time, actual duty factor of each gate signal are less than 0.5 in consideration of the dead time. As shown in Table 1, fo=22kHz and Td=2µs. Therefore the actual duty factor is about 0.456. On the other hand, the equation (8) can be also applied to the conventional full bridge inverter with series resonant load. In this case, Ed is the DC bus voltage that is converted from 3 phase utility voltage. Hence, in the proposed inverter, a square value of the DC bus voltage that is determined by the duty factor is a multiplying factor of the rated power to the conventional full bridge inverter.

According to the equation (5), the voltage of the DC bus capacitor is raised up to 1.83. As a result, it is expected that the rated power of this proposed inverter becomes about 3.35 times than the full bridge one. The simulation is implemented to evaluate the output power of the proposed inverter before the experiment. On the simulation, the output power of the proposed inverter is compared to the conventional full bridge inverter in a same condition shown in table. 1.

Table 2 shows the simulation results. Result the output power of the proposed inverter is obtained about 3.25 times compared with the conventional one in the simulation. Fig. 6 shows a simulated output voltage v_o and a output load current i_o.

Table 2: Simulation results of output power

	Unit	Proposed inverter	Full bridge inverter
Simulated power	W	1430	439

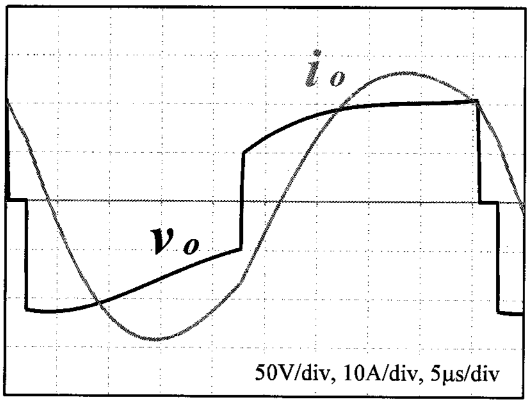

Fig. 6: The simulated output voltage and current waveforms

Next, scale modes of proposed inverter and the conventional full bridge inverter were tested to compare with the output power in a similar way of simulation. The experiment conditions of scale models are same as Table 1. The input voltage Ein is set at DC 50V that 3 phase utility voltage is converted by a diode rectifier through an autotransformer.

The observed waveforms of the proposed inverter are shown in Fig. 7. A black line is the output voltage waveform and a gray line is the output load current waveform. It is confirmed that the observed waveforms are similar to the simulation results. The surge voltage is observed when Sa and S1 turn off. This reason is thought that there is a small stray inductor between the output diode Da and the DC bus capacitor Cd in the scale model. The negative surge voltage is occurred across the stray inductor when the current starts flowing through Da after turning off Sa. As a result the positive surge voltage is occurred across the output terminal of the inverter. In the experiment results, the output load current of the proposed inverter was 19.8A and the output power was 1.42kW.

On the other hand, the conventional full bridge inverter output 11.2A as the load current in the same condition. The output power is obtained about 0.45kW. Therefore the proposed inverter achieved about 3.2 times power than the conventional one in this scale model experiment. Hence it was verified that the proposed inverter has superiority for high power induction heating applications.

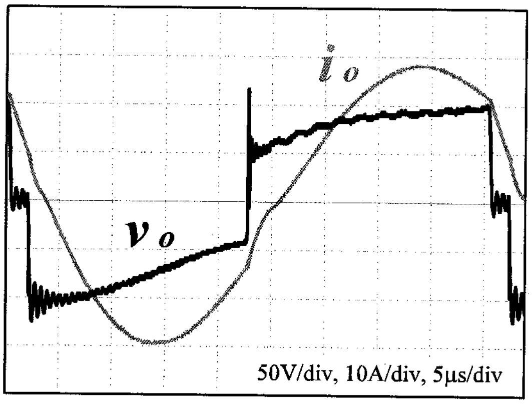

Fig. 7: The observed output voltage and current waveforms of scale model
(Input DC voltage: 50.0V, Inverter output voltage: 84.01V, Output load current: 19.84A, Output power: 1416W, Operation frequency: 22.08kHz)

5. Conclusion

This paper proposed a new high frequency inverter for induction heating applications which is required to output high power even in low input voltage condition. The proposed inverter has a boost chopper function in it and the voltage of DC bus capacitor can be raised than the input DC voltage. On the other hand, it can be said that the proposed inverter's operation is same as the conventional full bridge inverter's one from the view point of the output voltage waveform because its output voltage is the AC square waveform. Thus, the operation of the proposed inverter is explained that the pseudo-full bridge inverter operates under a high DC voltage that is raised up by the boost chopper function.

As a result, the proposed inverter obtains high output power than the conventional one in a same load condition. This paper discussed the circuit design so that S1 and S2 achieve ZVS turn-on condition by the current resonance. In addition, an adjustment way of the load equivalent resistance was described with some formula in order to obtain the requested output power. The rated output power is determined by the output load current phase difference to the voltage, the load equivalent resistance, the input DC voltage that is converted from the utility voltage, and the duty factor of Sa.

Especially, the duty factor has influence for the proposed inverter's power. It was confirmed that its relation well accorded with a simulation result. Experiment was implemented to demonstrate the principle of the proposed inverter operation by using the scale model. The observed waveforms had a good accord with the simulation results.

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